

**IN THE SPECIFICATION**

**Please replace paragraph [0043] with the following paragraph:**

**[0043]** Register bank 130 receives phase-4 clock signals. During phase 4, a register 134 addressed by select register[[ 134]] 160 is updated. For one embodiment, this involves sending data that is processed by bus controller 142 and held in transfer register 146 to the addressed register 134.